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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,161	09/26/2003	Christopher K. Y. Chun	SC12931TC	8118
23125	7590	12/13/2005	EXAMINER	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			WANG, ALBERT C	
			ART UNIT	PAPER NUMBER
			2115	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/672,161	Applicant(s) CHUN ET AL.	
	Examiner Albert Wang	Art Unit 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1,2,10-15,23 and 24 is/are rejected.
- 7) ☒ Claim(s) 16-22 and 25-27 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>9/04 & 4/04</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

1. Original claims 1-27 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said first standby signal" in the last line. There is insufficient antecedent basis for this limitation in the claim. Claims 2-9 depend on claim 1.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2 and 10-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Garcia et al., U.S. Patent No. 6,691,235 ("Garcia").

As per claim 1, Garcia discloses a data processing system, comprising:

a power management unit (fig. 1, DC/DC converter 14);

a first processor coupled to said power management unit (CPU 10);

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a voltage control module coupled to said power management unit and said first processor for selecting a first voltage level (decode logic 18), said voltage control module providing a first control signal and a second control signal to indicate said first voltage level to said power management unit (first and second programming inputs 16), said power management unit providing a first supply voltage corresponding to said first voltage level to said first processor in response to receiving said first control signal (providing V_{CORE}; col. 7, lines 36-62; col. 8, line 54 – col. 9, line 2).

As per claim 2, Garcia discloses said first processor provides a first voltage level request to said voltage control module (fig. 1, V2.2REQ).

As per claim 10, Garcia discloses a data processing system, comprising:

a first processor (fig. 1, CPU 10);

a voltage control module coupled to said first processor, wherein said voltage control module receives at least one desired voltage level indicator from said first processor (decode logic 18 receives indicators from CPU 10) and, based on the at least one desired voltage level indicator from said first processor, provides a first control signal and a second control signal indicating a first supply voltage level to be provided to the first processor (provides first and second programming inputs 16; col. 7, lines 36-62; col. 8, line 54 – col. 9, line 2).

As per claim 11, Garcia discloses the at least one desired voltage level indicator from said first processor comprises a first sleep mode indicator and a first requested voltage level provided by the first processor (col. 7, lines 36-62).

As per claim 12, Garcia discloses said first control signal is based on said first sleep mode indicator and said first requested voltage level, and said second control signal is based on said first sleep mode indicator (col. 8, line 54 – col. 9, line 2).

As per claim 13, Garcia discloses a voltage regulator, which provides said first supply voltage to said first processor (fig. 1, DC/DC converter 14 is a voltage regulator).

As per claim 14, Garcia discloses said voltage regulator is capable of being optimized based on at least one of said first control signal and said second control signal (col. 8, lines 8-19).

As per claim 15, Garcia discloses control storage circuitry, which stores said first requested voltage level (col. 8, lines 20-47).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Helms, U.S. Patent No. 6,748,545.

As per claim 23, Helms teaches a method of generating supply voltage in a data processing system having a first processor, comprising:

receiving a first sleep mode indicator (fig. 2, CPUSTOP#);

receiving a first voltage level indicator indicating a first voltage level (VID);

providing a first standby signal based on said first sleep mode indicator

(SELECT_VID#);

providing a first control signal based on said first voltage level indicator and said first sleep mode indicator (MVID); and

providing a first supply voltage to said first processor based on said first control signal and said first standby signal (CPUVCC).

However, Helms does not expressly teach said first sleep mode indicator is sent from said first processor. It is well known in the art to control a computer's power mode from the operating system or BIOS, which in turn run on the computer's processor. Therefore at the time of the invention, it would have been obvious to one of ordinary skill in the art that Helms' first processor is capable of sending a first sleep mode indicator.

As per claim 24, Helms teaches said first supply voltage has a voltage level different from said first voltage level (VID is a multi-bit digital value comprising high and low voltage levels whereas CPUVCC is converted from AC adapter voltage).

Allowable Subject Matter

8. Claims 16-22 and 25-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

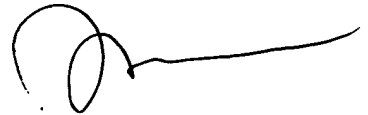
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AW

A handwritten signature in black ink, consisting of a stylized 'A' followed by a horizontal line.